S.No. 1879 **12UEL06**

(For the candidates admitted from 2012-2013 onwards)

B.Sc. DEGREE EXAMINATION, NOVEMBER 2017.

Fifth Semester

Electronics and Communication

ICs AND THEIR APPLICATIONS

Time : Three hours Maximum : 75 marks

PART A — ($10 \times 2 = 20$ marks)

Answer ALL questions.

1. List the basic processes used in silicon planar technology.

2. Define sheet resistance R_s.

3. What do you mean by Fan-out of a logic gate?

4. Define the term : Figure of merit of a logic gate.

5. What is an op.amp?

6. Define slew rate of an op.amp.

7. What are the modes of operation of a timer?

8. List any four important features of the 555 timer.

9. Metion the basic building blocks of a PLL.

10. What is the major difference between digital and analog PLLs?

PART B — (5 × 5 = 25 marks)

Answer ALL questions.

11. (a) Describe the diffusion process with a neat sketch.

Or

(b) Explain the term : Metallization.

12. (a) Explain the operation of DTL gate with a circuit.

Or

(b) Compare logic families.

13. (a) Explain the characteristics of an ideal op.amp.

Or

(b) Describe the working of integrator circuit using op.amp.

14. (a) Discuss the operation of a FSK generator using 555 timer.

Or

(b) Explain the working of missing pulse detector using 555 timer.

15. (a) With a suitable diagram, explain the working of FM detector using PLL.

Or

(b) Describe the operation of PLL FSK detector circuit.

PART C — (3 × 10 = 30 marks)

Answer any THREE questions.

16. Discuss the various ways for fabricating monolithic transistors.

17. Explain the working of standard TTL gate and discuss its transfer characteristics.

18. With suitable sketches, explain the operation of I to V converter using op.amp.

19. Draw and explain the functional diagram of a 555 timer.

20. With a suitable block diagram, explain the basic principle of Phase-Locked Loop (PLL).

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