S.No. 26 **12PELZ03**

(For the candidates admitted from 2012–2013 onwards)

M.Sc. DEGREE EXAMINATION, NOVEMBER 2017.

Third Semester

Electronics and Communication

VLSI DESIGN AND VHDL PROGRAMMING

Time : Three hours Maximum : 75 marks

SECTION A — (5 × 5 = 25 marks)

Answer ALL questions.

1. (a) Explain the operation of MOS transistor with a neat diagram.

Or

(b) Write a short note on epitaxy.

2. (a) Discuss about the history and development of VHDL.

Or

(b) What do you mean by identifiers? Explain it with an example.

3. (a) With a syntax and example, explain the concept of entity declaration.

Or

(b) Write the syntax and example for *exit* statement and explain.

4. (a) Write a short note on multiple drivers.

Or

(b) Write a VHDL coding for full adder using behavioral modeling style.

5. (a) Explain the concept of sub programs with an example.

Or

(b) What do you mean by attributes in VHDL? Explain.

SECTION B — (5 × 10 = 50 marks)

Answer ALL questions.

6. (a) Explain the following (i) oxidation (ii) Ion implantation and (iii) Diffusion.

Or

(b) With a neat diagram, explain the various steps involved in fabricating the CMOS IC using n-well process method.

7. (a) Explain in detail the various data objects available in VHDL with syntax and example.

Or

(b) Describe the concept of scalar data types with an example.

8. (a) Explain the *loop* statement with a syntax and example.

Or

(b) With a syntax and example, explain the *assertion* statement.

9. (a) Explain in detail the concept of unaffected value with an example.

Or

(b) Write a VHDL program for 1-to-4 decoder using behavioral modeling style.

10. (a) Explain in detail the concept of configuration declaration with an example.

Or

(b) With an example, explain the concept of package declaration and package body.

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