S.No. 23

(For the candidates admitted from 2012–2013 onwards)

M.Sc. DEGREE EXAMINATION, NOVEMBER 2017.

Third Semester

Electronics and Communications

DIGITAL SIGNAL PROCESSING

Time : Three hours   Maximum : 75 marks

PART A — (5 × 5 = 25 marks)

Answer ALL questions.

1. (a) Discuss about structures for linear phase FIR system.

Or

    (b) With necessary example, explain about limit cycles due to overflow.

2. (a) With a neat diagram, explain flow graph of a 2 point DFT.

Or

    (b) Discuss about efficient computation of the DFT.

3. (a) Compare Hamming and Bartlett windowing methods.

Or

(b) Discuss about the properties of commonly used windows.

4. (a) Write short notes on round off errors in FFT algorithm.

Or

(b) Explain about quantization of floating point number.

5. (a) List the key features of TMS320C5X digital signal processor.

Or

(b) Discuss about POP, POPD, PUSH and PSHD instructions.

PART B — (5 × 10 = 50 marks)

Answer ALL questions.

6. (a) Explain about network structures of FIR systems.

Or

(b) Describe about direct form and cascade form structures for IIR systems.

7. (a) Describe in detail decimation in time algorithm.

Or

(b) Explain Chrip transform algorithm with an example.

8. (a) Describe the designing of FIR filter by windowing method.

Or

(b) Discuss in detail about frequency transformation of low pass IIR filers.

9. (a) Analyze co-efficient quantization effects in FIR filters.

Or

(b) Describe about noise analysis A/D conversion.

10. (a) Draw the functional block diagram of TMS320C5X and explain its each block.

Or

(b) Describe about various types of instruction set in TMS320C5X.

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